CLAIMS

What is claimed is:

1. An apparatus, comprising:

a first end of a via disposed in a semiconductor support layer, the first end having a first diameter; and

a second end of the via having a second diameter, the first diameter greater than the second diameter.

2. The apparatus of claim 1 wherein the via includes a shaft between the first end and the second end, the shaft having a shaft diameter similar to the second diameter.

3. The apparatus of claim 1 wherein the first end forms a semi-cone in the semiconductor support layer.

4. The apparatus of claim 1, further comprising a dielectric layer disposed proximate to the semiconductor support layer, the via to pass through the dielectric layer.

5. The apparatus of claim 4 wherein a diameter of the via in the dielectric layer is similar to the first diameter.

6. The apparatus of claim 4, further comprising a contact disposed on the dielectric layer and electrically coupled to the via.

7. The apparatus of claim 1 wherein the via includes a metal-filled via.

8. A method, comprising:

dry etching a semiconductor support layer to a dialectic layer of a die to define a via hole in the semiconductor support layer, the via hole having a first end associated with the dielectric layer; and

dry etching the semiconductor support layer at the first end to define an enlarged end at the first end of the via hole.

9. The method of claim 8 wherein the enlarged end having a first diameter and the via hole having a second diameter, the first diameter greater than the second diameter.

10. The method of claim 8 wherein dry etching the semiconductor support layer to define the via hole and dry etching the semiconductor support layer to define the enlarged end is completed in a single dry etch process.

11. The method of claim 8, further comprising dry etching the dielectric layer to continue the via hole through the dielectric layer to a conductive layer disposed proximate to the dielectric layer.

12. The method of claim 11 wherein dry etching the dielectric layer is performed with a tool used in dry etching the semiconductor support layer.

13. The method of claim 11 wherein a diameter of the via hole in the dielectric layer is similar to a diameter of the enlarged end.

14. The method of claim 8, further comprising wet etching the dielectric layer to continue the via hole through the dielectric layer to a conductive layer disposed proximate to the dielectric layer.

15. The method of claim 8, further comprising aligning a dry etching tool with a conductive layer coupled to the dielectric layer before dry etching the semiconductor support layer to define the via hole.

16. The method of claim 8 wherein dry etching the semiconductor support layer to define the enlarged end comprises creating a charge on the dielectric layer to repel ions laterally to define the enlarged end in the semiconductor support layer.

17. The method of claim 16, further comprising adjusting a diameter of the enlarged end by adjusting an amount of time the ions are allowed to etch laterally from a center of the via hole.

18. The method of claim 8, further comprising:

etching the dielectric layer to continue the via hole through the dielectric layer to a conductive layer disposed proximate to the dielectric layer; and

filling the via hole and the enlarged end with a conductive material to form a via.

19. The method of claim 18, further comprising connecting the via to the conductive layer.

20. A die package, comprising:

a semiconductor support layer including a via having a first end and a second end in the semiconductor support layer, wherein a diameter of the first end is greater than a diameter of the second end;

a dielectric layer disposed proximate to the semiconductor support layer wherein the via passes through the dielectric layer; and

a contact disposed on the dielectric layer, the via coupled to the contact.

21. The die package of claim 20 wherein the via includes a shaft between the first end and the second end, a diameter of the shaft similar to the diameter of the second end.

22. The die package of claim 20 wherein the first end is a semi-cone shape centered on the via.

23. The die package of claim 22 wherein a diameter of the via through the dielectric layer is similar to a diameter of the semi-cone shape.

24. A system, comprising:

a printed circuit board (PCB); and

a processor coupled to the PCB, wherein the processor includes:

a semiconductor support layer including a via having a first end and a second end in the semiconductor support layer, wherein the first end having a first diameter and the second end having a second diameter, the first diameter greater than the second diameter;

a dielectric layer disposed proximate to the semiconductor support layer wherein the via passes through the dielectric layer; and

a contact disposed on the dielectric layer, the via coupled to the contact.

25. The system of claim 24 wherein the via includes a shaft between the first end and the second end, the shaft having a shaft diameter similar to the second diameter.

26. The system of claim 25 wherein the first end tapers outward from a center of the via within the semiconductor support layer towards the dielectric layer, the first end defining a semi-cone shape in the semiconductor support layer.

27. The system of claim 24 wherein the first diameter is approximately twice the second diameter.